Listing of the Claims

This listing of claims will replace all prior versions, and listings, of the claims:

1. (currently amended) A memory device comprising:

a magneto-resistive random access memory (MRAM);

a cache comprising a volatile memory;~~and~~

a decoder configured to translate referenced addresses to physical addresses to access data and pass the data between the MRAM and the cache and between the cache and a controller; and

an error detection and correction circuit electrically coupled to the cache and the MRAM, wherein the cache, the MRAM, the error detection and correction circuit, and the decoder are fabricated on a single semiconductor substrate.

2. (original) The memory device of claim 1, wherein the decoder translates referenced addresses from the controller to physical addresses in the MRAM and the cache.

3. (canceled)

4. (original) The memory device of claim 1, wherein the cache comprises static random access memory.

5. (original) The memory device of claim 1, wherein the cache comprises dynamic random access memory.

6. (canceled).

7. (original) The memory device of claim 1, wherein the cache comprises one of a unified cache and a segmented cache.

8. (original) The memory device of claim 7, wherein the segmented cache comprises a data segment and an instructions segment.

9. (currently amended) A memory device comprising:

a magneto-resistive random access memory (MRAM);

a volatile memory; ~~and~~

error detection and correction (ECC) circuit coupled to the MRAM; and

a virtual memory controller configured to pass data between the MRAM, the ECC circuit, the volatile memory, and a host, wherein the MRAM, volatile memory, and ECC circuit are provided on a single semiconductor chip.

10. (original) The memory device of claim 9, wherein the controller passes data between the volatile memory and the host based upon requests from the host.

11. (original) The memory device of claim 9, wherein the volatile memory comprises a static random access memory.

12. (original) The memory device of claim 9, wherein the volatile memory comprises a dynamic random access memory.

13. (original) The memory device of claim 9, wherein a portion of the MRAM comprises a page file.

14. (currently amended) A method for reading data or instructions from a memory device that comprises a magneto-resistive random access memory (MRAM) coupled to a cache comprising:

receiving a request from a controller to read data from the MRAM provided on a substrate;

determining if the requested data is located in the cache provided on the substrate;

passing the data from the MRAM to the cache if the data is not located in the cache; ~~and~~

passing the data to the controller from the cache; and

error correction decoding the data from the MRAM with a circuit provided on the substrate.

15. (canceled).

16. (original) The method of claim 14, wherein the request comprises reference addresses, the method further comprising:

translating the reference addresses to physical addresses.

17. (currently amended) A method for writing data to a memory device that comprises magneto-resistive random access memory (MRAM) coupled to a cache comprising:

receiving a request from a controller to write data to the MRAM provided on a substrate;

determining if a memory block where the data is to be stored is located in the cache provided on the substrate;

passing the memory block from the MRAM to the cache if the memory block is not located in the cache;

passing the data from the controller to the cache; ~~and~~

error correction encoding the data from the cache with a circuit provided on the substrate; and

passing the data from the cache to the MRAM.

18. (canceled).

19. (original) The method of claim 17, wherein the request comprises reference addresses, the method further comprising:

translating the reference addresses to physical addresses.

20. (currently amended) A portable electronic device comprising:

a processor; and

a semiconductor memory device comprising:

a magneto-resistive random access memory (MRAM);

an error detection and correction (ECC) circuit coupled to the MRAM;

a cache comprising a volatile memory; and

a control and address decoder configured to control the passing of data between the MRAM, the ECC circuit, and the cache and between the cache and the processor.

21. (original) The portable electronic device of claim 20, wherein the portable electronic device comprises a display.

22. (original) The portable electronic device of claim 20, wherein the portable electronic device is one of a personal digital assistant, a cellular telephone, a digital music player, a personal organizer, and a digital camera.